AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently amended): A split gate flash memory cell, comprising:

a substrate having a trench;

a conductive line ~~stud~~ disposed in a lower portion of the trench ~~the lower trench~~ and insulated from the substrate serving as a source line;

a source region formed in the substrate adjacent to an upper portion of the ~~upper~~ conductive line ~~stud~~;

an insulating layer disposed on the conductive line ~~stud~~;

a conductive spacer disposed on an upper sidewall portion of the trench ~~the upper sidewall of the trench~~ serving as a floating gate, protruding and insulated from the substrate;

a first insulating stud disposed on the insulating layer, with the top thereof higher than that of the conductive spacer;

a first conductive layer disposed over the substrate ~~of the outside~~ adjacent to the conductive spacer , serving as a control gate, the first conductive layer insulated from the conductive spacer and the substrate, respectively;

a first insulating spacer disposed on the sidewall of the insulating stud to cover the first conductive layer; and

a drain region formed in the substrate ~~of the outside~~ adjacent to the first conductive layer.

Claim 2 (Original): The memory cell as claimed in claim 1, further comprising a second conductive layer disposed between the first conductive layer and the first insulating spacer.

Claim 3 (Original): The memory cell as claimed in claim 2, wherein the second conductive layer is tungsten silicide.

Claim 4 (Original): The memory cell as claimed in claim 1, further comprising a second insulating spacer disposed on the sidewall of the first conductive layer.

Claim 5 (Original): The memory cell as claimed in claim 4, wherein the first and second insulating spacers are silicon nitride.

Claim 6 (Original): The memory cell as claimed in claim 1, further comprising:

a conductive plug disposed on the drain region serving as a bit line contact;

a cap layer disposed over the insulating stud and the first insulating spacer; and

a third conductive layer serving as a bit line disposed on the conductive plug and the cap layer.

Claim 7 (Original): The memory cell as claimed in claim 6, wherein the conductive plug is doped polysilicon.

Claim 8 (Original): The memory cell as claimed in claim 6, wherein the cap layer is silicon oxide.

Claim 9 (Original): The memory cell as claimed in claim 6, wherein the third conductive layer is tungsten.

Claim 10 (Currently amended): The memory cell as claimed in claim 1, wherein the conductive line ~~stud~~ is polysilicon.

Claim 11 (Original): The memory cell as claimed in claim 1, wherein the insulating layer is high density plasma oxide.

Claim 12 (Original): The memory cell as claimed in claim 1, wherein the conductive spacer is doped polysilicon.

Claim 13 (Original): The memory cell as claimed in claim 1, wherein the insulating stud is silicon oxide or boron silicate glass.

Claim 14 (Original): The memory cell as claimed in claim 1, wherein the first conductive layer is polysilicon.

Claim 15 (Currently amended): A split gate flash memory cell, comprising:

a substrate having a trench;

a polysilicon line ~~stud~~ disposed in a lower portion of the trench ~~the lower trench~~ and insulated from the substrate serving as a source line;

a source region formed in the substrate adjacent to an upper portion of the ~~upper~~ polysilicon line ~~stud~~;

an insulating layer disposed on the polysilicon line ~~stud~~;

a polysilicon spacer disposed on an upper sidewall portion of the trench ~~the upper sidewall of the trench~~ serving as a floating gate, protruding and insulated from the substrate;

an insulating stud disposed on the insulating layer, with the top thereof higher than that of the polysilicon spacer;

a polysilicon layer disposed over the substrate ~~of the outside~~ adjacent to the polysilicon spacer, serving as a control gate, with the polysilicon layer insulated from the polysilicon spacer and the substrate, respectively;

a first insulating spacer disposed on the sidewall of the first insulating stud to cover the polysilicon layer;

a second insulating spacer disposed on the sidewall of the polysilicon layer; and

a drain region formed in the substrate ~~of the outside~~ adjacent to the polysilicon layer.

Claim 16 (Original): The memory cell as claimed in claim 15, further comprising a tungsten silicide layer disposed between the polysilicon layer and the first insulating spacer.

Claim 17 (Original): The memory cell as claimed in claim 15, wherein the first, second, and third insulating spacers are silicon nitride.

Claim 18 (Original): The memory cell as claimed in claim 15, further comprising:

a polysilicon plug disposed on the drain region serving as a bit line contact;

a cap layer disposed over the insulating stud and the first insulating spacer; and

a tungsten layer serving as a bit line disposed on the polysilicon plug and the cap layer.

Claim 19 (Original): The memory cell as claimed in claim 18, wherein the cap layer is silicon oxide.

Claim 20 (Original): The memory cell as claimed in claim 15, wherein the insulating layer is high density plasma oxide.

Claim 21 (Original): The memory cell as claimed in claim 15, wherein the first insulating stud is silicon oxide or boron silicate glass.